Sole Inventor

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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Kwan Ju Koh**, a citizen of Republic of Korea, residing at Geumgangmaeul 407-101, Jung 4-dong, Wonmi-gu, Bucheon-si, Gyeonggi-do, Korea have invented new and useful **SEMICONDUCTOR DEVICES AND METHODS FOR FORMING SEMICONDUCTOR DEVICES**, of which the following is a specification.

SEMICONDUCTOR DEVICES AND METHODS FOR FORMING SEMICONDUCTOR DEVICES

FIELD OF THE DISCLOSURE

[0001] This disclosure relates generally to semiconductor devices and, more particularly, to methods for forming semiconductor devices.

BACKGROUND

[0002] As semiconductor devices have become more highly integrated, the size of chips have decreased and the width of the polysilicon gates of the chips have become narrower.

[0003] A conventional method of forming a gate of a semiconductor device will now be described with reference to FIG. 1. A gate polysilicon layer is formed on a semiconductor substrate 11. Then, the gate polysilicon layer is selectively removed by an etching process using a photoresist pattern (not shown) to form a gate electrode 14.

[0004] A low concentration ion implantation process is performed to form LDD (lightly doped drain) regions 13. A nitride film is formed on top of the entire structure wherein the gate electrode 14 is formed. Then by etching the nitride film, the nitride film on side surfaces of the gate electrode 14 is left as sidewalls 15 of the gate electrode 14.

[0005] Impurity ions are implanted into the LDD regions 13 on both sides of the gate electrode 14 to form source/drain regions 12. A material for forming a silicide layer (e.g., metal) is deposited on a top surface of the entire

structure and then an annealing process is performed to form a silicide layer 16 on the exposed surfaces.

[0006] In the conventional gate forming method as described above, as the size of the chip becomes smaller, the width of the polysilicon gate becomes narrower, and, as the polysilicon gate becomes narrower, the silicide resistance increases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Fig. 1 is a cross-sectional view of a semiconductor device formed by a conventional process.

[0008] Figs. 2A to 2I depict cross-sectional views of a semiconductor device being formed by the disclosed process.

DETAILED DESCRIPTION

[0009] As an overview, a semiconductor device may be formed by performing a lower gate electrode forming process and other ion implantation process. (These processes may affect the characteristics of the device.) Then, an upper gate electrode is formed by depositing a gate polysilicon layer on top of the entire structure wherein the lower gate electrode is formed and then etching the gate polysilicon layer. A silicide layer is then formed on both top and side surfaces of the upper gate electrode to increase the surface area of the silicide layer.

[0010] A preferred method of forming a gate in a semiconductor device will now be described in greater detail with reference to Figs. 2A to 2I.

[0011] Referring to Fig. 2A, a lower gate polysilicon layer 102 is formed on a semiconductor substrate 101 and a photoresist layer is coated thereon. At this time, the thickness of the lower gate polysilicon layer 102 is about 800~1000 angstrom.

[0012] Referring to Fig. 2B, using a patterned photoresist layer 110, the lower gate polysilicon layer 102 is selectively removed by an etching process to form a lower gate electrode 102a.

[0013] Referring to Fig. 2C, LDD regions 103 are formed on opposite sides of the lower gate electrode 102a through a conventional low concentration ion implantation process.

[0014] Referring to Fig. 2D, a nitride film 104 is formed on top of the entire structure of the semiconductor substrate wherein the lower gate electrode 102a is formed (i.e., on top of the entire structure shown in Fig. 2C).

[0015] Referring to Fig. 2E, in an etching process of the nitride film 104, by over-etching, the nitride film 104 on the side surfaces of the lower gate electrode 102a are left as sidewalls 104a of the lower gate electrode 102a and the nitride film 104 on the top of the lower gate electrode 102a is totally removed.

[0016] Referring to Fig. 2F, source and drain regions 105 are formed by implanting impurity ions into the LDD regions 103 on opposite sides of the lower gate electrode 102a.

[0017] Referring to Fig. 2G, an upper gate polysilicon layer 106 is formed on top of the entire structure wherein the source and drain regions 105

are formed (i.e., on top of the entire structure shown in Fig. 2F). A photoresist layer 107 is then coated thereon.

[0018] Referring to Fig. 2H, after patterning the photoresist layer 107, the upper gate polysilicon layer 106 is selectively removed through an etching process to form an upper gate electrode 106a. In this way, a gate electrode including the upper and the lower gate electrodes 102a, 106a is completed.

[0019] Referring to Fig. 2I, after a material for forming a silicide layer 108 (e.g., metal) is deposited on top of the entire structure wherein the upper gate electrode is formed, a silicide layer 108 is formed on the exposed surfaces by an annealing process. Specifically, the silicide layer 108 is formed on the top and side surfaces of the upper gate electrode 106a and the top surfaces of the source and drain regions 105. Since the silicide layer 108 is formed on the side surfaces of the upper gate electrode 106a as well as on the top surface thereof, the surface area of the silicide layer 108 is increased in comparison with the silicide layers of semiconductor devices formed by conventional processes wherein the silicide layer 16 is not formed on the side surfaces of the gate electrode 14 (see Fig. 1). Therefore, the resistance of the silicide layer 108 of the device of Fig. 2I is minimized.

[0020] From the foregoing, persons of ordinary skill in the art will appreciate that stable control of the semiconductor device can be obtained by increasing the surface area of the silicide layer 108 to minimize silicide resistance. Further, the thickness of the lower gate electrode 102 can be adjusted so that patterning of PR and BARC (bottom anti-reflection coating)

of a small thickness is possible, thereby allowing the teachings of the present disclosure to be applied to fine patterning processes.

[0021] From the foregoing, persons of ordinary skill in the art will appreciate that semiconductor devices and methods for forming semiconductor devices have been disclosed wherein a gate electrode is formed with an upper and a lower gate electrode and a silicide layer is formed on both top and side surfaces of the upper gate electrode to increase the surface area of the silicide layer, thereby minimizing the silicide resistance.

[0022] In a disclosed method, a gate of a semiconductor device is formed by: forming a lower gate polysilicon layer on a semiconductor substrate; selectively removing the lower gate polysilicon layer to form a lower gate electrode; forming LDD regions on opposite sides of the lower gate electrode; forming sidewalls of the lower gate electrode; forming source and drain regions on opposite sides of the lower gate electrode; forming an upper gate polysilicon layer on top of the entire structure; selectively removing the upper gate polysilicon layer to form an upper gate electrode; and forming a silicide layer on top and side surfaces of the upper gate electrode.

[0023] Preferably, the silicide layer is formed by depositing a material for forming the silicide layer on top of entire structure in which the upper gate electrode is formed and executing an annealing process to form the silicide layer on exposed surfaces of the entire structure.

[0024] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of

manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.